REMARKS

The Examiner objected to the abstract of the disclosure because it fails to comply with the proper language and format. In response, Applicants have supplied a replacement abstract.

The amendment of the specification does not add new matter as the amendment is based on U.S. 5,961,653 which has been incorporated by reference and particularly on col. 3, lines 36-39 which states " Referring to FIG. 1, the present invention is preferably embodied in an integrated circuit chip 100 having logic 104 and 106, a DRAM 102 embedded in the logic, and a BIST macro (not shown) for testing the DRAM."

The amendment of claims 2-6 are made to clarify antecedent basis and are not made in response to the Examiner rejections of claims 2-6.

The Examiner rejected claims 1-6 under 35 U.S.C. § 102(e) as allegedly being anticipated by Ochi (US 2003/0128045) Published: July 10, 2003, Filed: June 20, 2002.

The Examiner rejected claims 7-10 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ochi (US 2003/0128045) in view of Schwarz (U.S. Patent No. 6,496,947) Filed: October 25, 1999.

Applicants respectfully traverse the §102(e) and §103(a) rejections with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Ochi discloses a method of testing a plurality of semiconductor device under test (DUTs), such as DRAM blocks, each DUT connected to a test circuit, (see, Abstract and Figures 1 and 2), comprising: Generating a test pattern using a test pattern generator (ALPG 1), where the test pattern output is coupled to a driver circuit (21A, B...N), which produces a test signal corresponding to (DUTs 1, 2...N). Performing a write operation by sending a write signal into each DUT (DUTs 1, 2...N) through a corresponding driver circuit (21A, B ...N) in response to a test pattern output from the test pattern generator. Performing a pause for a predetermined period of time, using a timer (24A, B ..N) for setting a pause time and read time of each DUT and then performing a read operation by reading the resulting pattern from each OUT through a corresponding comparator (23A, B ...N) which compares the read signal with a predetermined reference value (not shown) and determines the DUT is defective or acceptable. The write operation is performed before the pause and the read operation is performed after the pause for the predetermined period of time, in Figure 2, which is a diagram showing the procedures for simultaneously subjecting to a pause test two DUTs. The pausing (t1-t2) of DUT 1 overlaps In time with the pausing (it-t4) of DUT 2."

Applicants contend that claim 1, as amended, is not anticipated by Ochi because Ochi does not teach each and every feature of claim 1. As a first example, Ochi does not teach or suggest "for each DRAM block comparing a data pattern based on said test data pattern to said resulting data pattern." Applicants respectfully point out that Ochi is comparing "a ratio of a read signal level to a write signal level" to a "predetermined level" and not comparing "a data pattern based on said test data pattern to said resulting data pattern" as Applicants claim 1 requires. See Ochi col. 2, paragraph 0018 which states in part " The memory device is then

determined to be defective or acceptable by means of checking whether or not a ratio of a read signal level to a write signal level is higher than a predetermined level; e.g, 80%." Further, the circuit illustrated in FIG. 1 of Ochi is only capable of measuring signal levels as element 21A is a driver circuit and element 23A is a determination circuit. See Ochi paragraph 22 which states in part "Reference numeral 23A designates a determination circuit which checks the level of a signal read from the DUT..."

As a second example Ochi does not teach "generating a test data pattern in a processor based built-in self test system, said built in self test system coupled to said embedded DRAM on a same integrated circuit chip." Applicants respectfully point out that Ochi teaches a test apparatus and not "built in self test system coupled to said embedded DRAM on a same integrated circuit chip" as Applicants claim 1 requires.

As a third example Ochi does not teach "said embedded DRAM comprised of DRAM blocks." Applicants respectfully point out that Ochi teaches that there is no teaching in Ochi that the DUTs are DRAM blocks of an embedded DRAM. In fact, Ochi's statements in Ochi paragraphs 19 and 28 indicate that the DUTs have different pause capability would and are separate memories not blocks of the same memory since the DRAM blocks of an embedded DRAM would have the same pausing capabilities.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Ochi and is in condition for allowance. Since claims 2-10 depend from claim 1, Applicants respectfully maintain that claims 2-10 are likewise in condition for allowance.

As to claims 3 and 6, the Examiner states that "Ochi discloses enabling simultaneous testing of a plurality of memory devices by performing a simultaneous write operation for each

DUT (DUT's 1, 2...N) through a corresponding driver circuit (21A, B ... N) in response to a test pattern output from the test pattern generator, and then performing a simultaneous read operation by reading the resulting pattern from each DUT through a corresponding comparator (23A, B ... N) which compares the read signal with a predetermined reference value (not shown) and determines the DUT is defective or acceptable. With respect to claimed feature of performing a write and a read operation sequentially from a first DRAM block to a last DRAM block of the multiplicity of DRAM blocks', Ochi recognizes that one may perform sequential write or read on one DRAM block at a time of plurality of memory devices, by describing a related-art tester for measuring memory devices of different capabilities on a one-by-one basis. However, measurement of memory devices on a per-device basis involves consumption of a very long measurement time. This results in a drop in processing capability, which in turn leads to a hike in testing costs, (see, Background Art)."

As to both claims 3 and 6, Applicants maintain that the Examiner has improperly rejected claims 3 and 6 under 102(e) because claims 3 and 6 are not "identically" disclosed as 35. U.S.C. 102 (e) requires and as required by MPEP 706.02(a) which states "for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Applicants maintain that the Examiners alleged teaching in the background of Ochi describes the prior art problem Ochi is trying to overcome and is not part of the invention of Ochi. It does not matter, under 35 USC 102 that the background of the reference may have some features lacking in the specification of the reference.

Applicants contend that claim 3 is not anticipated by Ochi because Ochi does not teach each and every feature of claim 3. As a first example Ochi does not teach "wherein said step of

performing said write of said test data pattern into said DRAM block is performed sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks."

As a second example, Ochi does not teach or suggest "the writing of a previous DRAM block of said multiplicity of DRAM blocks being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM blocks." Applicants respectfully point out neither reading "sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks" or "the writing of a previous DRAM block of said multiplicity of DRAM blocks being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM blocks" is taught by Ochi. Ochi actually teaches writing all DUTs simultaneously. (see Ochi Abstract paragraphs 7, 12, and FIG 2 and paragraphs 28 through 34 which describe FIG. 2).

Based on the preceding arguments, Applicants respectfully maintain that claim 3 is not unpatentable over Ochi and is in condition for allowance.

Applicants contend that claim 6 is not anticipated by Ochi because Ochi does not teach each and every feature of claim 6. As a first example Ochi does not teach "wherein said step of performing said read of said test data pattern into said DRAM block is performed sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks."

As a second example, Ochi does not teach or suggest "the reading of a previous DRAM block of said multiplicity of DRAM blocks being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM blocks." Applicants respectfully point out neither reading "sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks" or "the writing of a previous DRAM block of said multiplicity of DRAM blocks being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM

blocks" is taught by Ochi. Ochi actually teaches reading all DUTs simultaneously (see Ochi Abstract paragraphs 7, 12, and FIG 2 and paragraphs 28 through 34 which describe FIG. 2).

Based on the preceding arguments, Applicants respectfully maintain that claim 6 is not unpatentable over Ochi and is in condition for allowance.

35 USC § 103 Rejections

As to claims 7, 8 and 9, the Examiner states that "Ochi substantially discloses the claimed invention as described in claim 1, including comparators (23A, B ... N) for each DUT, which compare the read signal with a predetermined reference value (not shown) and determine the corresponding DUT is defective or acceptable. Ochi does not explicitly disclose, 'determining redundancy allocation information based on said resulting data pattern; and storing said redundancy allocation information for each said DRAM in separate registers, the storing of any previous redundancy allocation information for a previous DRAM block of said multiplicity of DRAM blocks being completed before the storing of subsequent redundancy information for a subsequent DRAM block of said multiplicity of said DRAM blocks, wherein the number of the registers is equal to the number of said DRAM blocks, and wherein the registers are coupled in series and further including scanning out each register sequentially'. However, in analogous art, Schwarz discloses a method of inserting a pause within a GIST [BIST] test algorithm implemented by the BISR [BIST] circuit in Figure 1, as illustrated by the flow chart of Figure 6. At step 404, compare circuit 28 compares the state read from the cell with the expected state. At step 405, if there is an error, address re-map circuit 26 replaces the cell (or row containing the cell) with a redundant cell (or row). If the cell cannot be replaced, fail flag 44 is activated. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an address re-map circuit 26 as taught by Schwarz in the semiconductor device CUT of Ochi, for the purpose of repairing the DUT by replacing a defective cell (or row containing the defective cell) with a redundant cell (or row). A person skilled in the art would have been motivated to do so, since it is cost effective to repair expensive memory devices before disposal."

Applicants contend that claim 7 is not obvious in view of Ochi in view of Schwarz because Ochi in view of Schwarz does not teach or suggest every feature of claim 7. As a first example, Ochi in view of Schwarz does not teach or suggest "storing said redundancy allocation information for each said DRAM in separate registers" Applicants respectfully maintain out that that neither Ochi or Schwarz teach "storing said redundancy allocation information" in registers, no less "storing said redundancy allocation information for each said DRAM in separate registers" as Applicants claim 7 requires. Applicants point out the detailed structure and mode of operation of ADDR REMAP 26 of FIG. 1 of Schwarz is not taught and appears to be a circuit for locating unused redundancy addresses (and not a register) for altering the ADDR DECODE 24 controlling RAM 12. (see Schwarz, col. 3, lines 24-27, col 4, lines 44-52)

As a second example, Ochi in view of Schwarz does not teach or suggest "storing of any previous redundancy allocation information for a previous DRAM block of said multiplicity of DRAM blocks being completed before the storing of subsequent redundancy information for a subsequent DRAM block of said multiplicity of said DRAM blocks."

Based on the preceding arguments, Applicants respectfully maintain that claim 7 is not unpatentable over Ochi in view of Schwarz and is in condition for allowance.

Applicants contend that claim 8 is not obvious in view of Ochi in view of Schwarz because Ochi in view of Schwarz does not teach or suggest every feature of claim 8. As a first example, Ochi in view of Schwarz does not teach or suggest "wherein the number of said registers is equal to the number of said DRAM blocks." Applicants can find no teaching in either Ochi or Schwarz that "the number of said registers is equal to the number of said DRAM blocks" and respectfully request the Examiner point to the specific teaching.

Based on the preceding arguments, Applicants respectfully maintain that claim 8 is not unpatentable over Ochi in view of Schwarz and is in condition for allowance.

Applicants contend that claim 9 is not obvious in view of Ochi in view of Schwarz because Ochi in view of Schwarz does not teach or suggest every feature of claim 9. As a first example, Ochi in view of Schwarz does not teach or suggest "said registers are coupled in series." As a second example, Ochi in view of Schwarz does not teach or suggest "scanning out each register sequentially. Applicants can find no teaching in either Ochi or Schwarz that "said registers are coupled in series and further including scanning out each register sequentially" and respectfully request the Examiner point to the specific teaching.

Based on the preceding arguments, Applicants respectfully maintain that claim 9 is not unpatentable over Ochi in view of Schwarz and is in condition for allowance.

As to claim 10, the Examiner states that "with respect to claimed fuse delete information, Ochi [Schwarz]discloses an address re-mapping circuit 26, which receives the selected address from multiplexer 21 and, based on the address, re-maps the selected row to avoid faulty memory cells in memory array 12. Address re-map circuit 26 selectively drives redundant word lines 98 to avoid the faulty memory cells, as is known in the art." Applicants contend that claim 10 is not obvious in view of Ochi in view of Schwarz because Ochi in view of Schwarz does not teach or suggest every feature of claim 10. For example, Ochi in view of Schwarz does not teach or suggest "writing back fuse delete information based on said redundancy allocation information into said registers." Applicants can find no teaching in either Ochi or Schwarz of "fuses," of "fuse delete information" or of "writing back fuse delete information... into said registers." In

fact, Schwarz would not require fuses to encode redundancy location information because ADDR REMAP 26 appears to perform that function. Applicants respectfully request the Examiner point to the specific teaching.

Based on the preceding arguments, Applicants respectfully maintain that claim 10 is not unpatentable over Ochi in view of Schwarz and is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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Dated: 12/02/2005

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